

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re Application of

Takahashi, Hiroshi

Serial No. **09/884,662**

Filed: **06/19/2001**

For: **SEMICONDUCTOR CIRCUIT**



Docket No.: **TI-29232**

Art Unit: **2819**

Examiner: **Chang, Daniel**

Conf. No.: **4499**

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AMENDMENT TRANSMITTAL FORM

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8(a)

I hereby certify, that on this date, this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner of Patents and Trademarks, Washington, DC 20231.

Elizabeth Austin

Date

June 17, 2002

Assistant Commissioner For Patents

Washington, D.C. 20231

Sir:

Transmitted herewith is an amendment in the above-identified application.

The fee has been calculated as shown below:

CLAIMS AS AMENDED						
	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE	ADDITIONAL FEE
Total Claims	27	Minus	20	0	x \$18 =	\$ 0.00
Independent Claims	3	Minus	3	0	x \$84 =	\$ 0.00
TOTAL ADDITIONAL FEE						\$ 0.00

Charge the total additional fee, and any further fees, or credit overpayment to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. An original and two copies of this sheet are enclosed.

Texas Instruments Incorporated
P. O. Box 655474, M/S 3999
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AMENDMENT - 37 CFR § 1.111

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

<u>MAILING CERTIFICATE UNDER 37 CFR § 1.8(a)</u>	
I hereby certify that the above correspondence is being deposited with the U.S. Postal Service as first class mail in an envelope addressed to: Assistant Commissioner of patents and Trademarks, Washington, DC 20231.	
 Elizabeth Austin	<u>6-17-02</u> Date

Responsive to the Office Action dated March 18, 2002, please amend the above-identified application as follows:

IN THE SPECIFICATION – (clean version):

Please change the Title of the Invention from “Semiconductor Circuit” to --High Speed Semiconductor Circuit Having Low Power Consumption--.

Please delete the Abstract and replace with the following:

--A semiconductor circuit which can restrain increase in manufacturing cost and layout area to a minimum level and can realize high speed and low power consumption. Bias

A1